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US Patent No. 5,342,806

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PATENT & TRADEMARK OFFICE

Attorney Docket No. 81753.0079
Customer No. 26021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 5,342,806
Michio ASAHINA
Serial No: 07/780,455
Filed: October 22, 1991
For: Method for Fabricating a Semiconductor Device having a Conductor Structure with a Plated Layer

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Certificate
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of Correction

Dear Sir:

Transmitted herewith in the above-identified patent are the following:

- ☒ Request for Expedited Issuance of Certificate of Correction.
- ☒ Certificate of Correction form PTO/SB/44.
- ☒ Exhibits A-F.
- ☒ Return Postcard.
- ☒ The Commissioner is hereby authorized to charge any deficiencies of fees associated with this communication or credit any overpayment to Deposit Account No. 50-1314. A copy of this sheet is enclosed.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: July 28, 2006

By: ______________________
Troy M. Schmelzer
Registration No. 36,667
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Telephone: 213-337-6700
Facsimile: 213-337-6701

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 5,342,806

Michio ASAHINA

Issued: August 30, 1994

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Signature Date

REQUEST FOR EXPEDITED ISSUANCE OF CERTIFICATE OF CORRECTION

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Correction of the captioned patent under 37 CFR 1.322 and MPEP 1480 is requested.

The text of the requested correction is set forth on the enclosed Certificate of Correction form (PTO/SB/444). The error in the captioned patent was incurred through the fault of the Office, the matter is clearly disclosed in the records of the Office, and this Request is accompanied by documentation that unequivocally supports the patentee's assertion that correction is needed. Accordingly, applicant has met the requirements for an expedited issuance of a Certificate of Correction under MPEP 1480.01 and respectfully requests same.

The errors in need of correction are in the text of claims 1 and 2 of the patent. Applicant has discovered that amendments made during prosecution and approved by the Examiner were not correctly entered into the claims of the issued patent. Issued claims 1 and 2 correspond to prosecuted claims 25 and 27 that were added as new claims in an amendment dated November 25, 1992 (Exhibit A). The original

text of new claims 25 and 27, as added to the application on November 25, 1992, is set forth below. For purposes of later discussion, claims 25 and 27 are set forth below with lines numbered and with the same line divisions (i.e., each line has the same text) as in the November 25, 1992 amendment.

	Claim 25 (added on November 25, 1992)
1	25. A method of fabricating a semiconductor device,
2	comprising the steps of:
3	providing a substrate having a doped
4	semiconductor region and a gate wiring, forming a lower
5	conductor structure, and forming an insulating layer
6	overlying said lower structure and having at least one
7	through opening extending to said lower conductor
8	structure; and
9	forming an upper conductor structure on the
10	insulating layer and causing the upper conductor
11	structure to be connected to the lower conductor
12	structure via the through opening;
13	wherein each said step of forming a conductor
14	structure is carried out by:
15	forming at least one layer of a metal, a
16	metal silicide, a metal nitride, a metal carbide, or a
17	conductive oxide film; and
18	performing a plating operation in order to
19	form a metal plating layer on the at least one layer, so
20	that the metal plating layer adheres to the at least one
21	layer.
	Claim 27 (added on November 25, 1992)
1	27. A method of fabricating a semiconductor device,
2	comprising the steps of:
3	providing a substrate having a doped
4	semiconductor region, a gate wiring, a lower conductor
5	structure, and an insulating layer overlying said lower
6	structure and having at least one through opening
7	extending to said lower conductor structure; and
8	forming an upper conductor structure on the
9	insulating layer and causing the upper conductor
10	structure to be connected to the lower conductor
11	structure via the through opening;
12	wherein said step of forming an upper conductor
13	structure is carried out by:

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14	forming at least one layer of a metal, a
15	metal silicide, a metal nitride, a metal carbide, or a
16	conductive oxide film;
17	performing a plating operation in order to
18	form a metal plating layer on the at least one layer, so
19	that the metal plating layer adheres to the at least one
20	layer; and
21	after said step of performing a plating
22	operation, performing a thermal treatment in order to
23	diffuse material from the plating layer into the at least
24	one layer.

An office action finally rejecting claims 25 and 27 was mailed on January 4, 1993. In response, applicant filed an amendment under 37 CFR 1.116 on March 31, 1993. In the March 31 amendment, which is attached as Exhibit B, claim 25 was amended and claim 27 was not amended. The amendments to claim 25 are set forth below, again with line numbering and line divisions matching those in the March 31 amendment:

	Claim 25 (amended on March 31, 1993)
1	25. A method of fabricating a semiconductor
2	device, comprising the steps of:
3	providing a substrate having a doped semiconductor region
4	and a gate wiring, forming a lower conductor structure, and forming
5	an insulating layer overlying said lower structure and having at
6	least one through opening extending to said lower conductor
7	structure; and
8	forming an upper conductor structure on the insulating
9	layer and causing the upper conductor structure to be connected to
10	the lower conductor structure via the through opening;
11	wherein each said step of forming a conductor structure
12	is carried out by:
13	forming at least one layer of a metal, a metal
14	silicide, a metal nitride, a metal carbide, or a conductive oxide
15	film; and
16	performing a plating operation in order to form a
17	metal plating layer on the at least one layer, so that the metal
18	plating layer adheres to the at least one layer; and

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wherein said steps of forming a lower conductor structure and an upper conductor structure are carried out so that the at least one layer of the upper conductor structure contacts the metal plating layer of the lower conductor structure.

A Notice of Allowance, attached as Exhibit C, was mailed on April 16, 1993. The Notice of Allowance entered the March 31 amendment, and also included Examiner's amendments to claims 25 and 27 as follows:

Claim 25, line 4, after "structure", insert "which includes a metal plating layer".

Claim 25, line 5, after "structure", insert "and contacting metal plating layer,".

Claim 25, line 8, after "structure", insert "which also includes a metal plating layer".

Claim 25, line 16, change "form a" to "form the".

Claim 27, line 5, after "structure", insert "which includes a metal plating layer".

Claim 27, line 6, after "structure", insert "and contacting metal plating layer,".

It is clear that these line numbers refer to the line numbers of the most recent claim versions. In claim 25, for example, the first version of the claim (as added on November 25) does not include a "structure" in line 4 or a "form a" in line 16, as is required to carry out the Examiner's amendment. However, the lines of the second and latest version of claim 25 (as amended on March 31) correspond in all respects to the Examiner's amendment. There is only one version of claim 27 (as added on November 25), so the Examiner's amendment must apply to that version.

Applicant noticed two errors in the Examiner's amendment. Two of the proposed insertions lacked proper antecedent basis for "metal plating layer". To correct these errors, an amendment under 37 CFR 1.312 was filed on April 29, 1993 (Exhibit D). In the April 29 amendment, applicant requested that the Examiner's proposed insert at claim 25, line 5, be changed from --and contacting metal plating

layer,-- to --, and contacting the metal plating layer--, and that the Examiner's proposed insert at claim 27, line 6, be changed from --and contacting metal plating layer,-- to --, and contacting the metal plating layer--. A communication was mailed by the USPTO on September 2, 1993 indicating that the amendment under 37 CFR 1.312 was entered (Exhibit E).

The application subsequently issued as U.S. patent 5,342,806 on August 30, 1994 (Exhibit F). Set forth below for prosecuted claims 25 and 27 are the post-allowance amendments that <u>should have been made</u> in view of the Examiner's April 16 amendment and applicant's April 29 amendment, followed by issued claims 1 and 2 (corresponding to prosecuted claims 25 and 27) showing the amendments that were <u>actually made</u>.

Claim 25 (Showing Amendments that should have been Made)

25. A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region and a gate wiring, forming a lower conductor structure <u>which includes a metal plating layer</u>, and forming an insulating layer overlying said lower structure<u>, and contacting the metal plating layer</u> and having at least one through opening extending to said lower conductor structure; and

forming an upper conductor structure <u>which also includes a metal plating layer</u> on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

wherein each said step of forming a conductor structure is carried out by:

forming at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide, or a conductive oxide film; and

performing a plating operation in order to form ~~a~~ <u>the</u> metal plating layer on the at least one layer, so that the metal plating layer adheres to the at least one layer; and

wherein said steps of forming a lower conductor structure and an upper conductor structure are carried out so that the at least one layer of the upper conductor structure contacts the metal plating layer of the lower conductor structure.

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Issued Claim 1 (Showing Amendments that were actually Made)

1. A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region, and a gate wiring, forming a lower conductor structure, and contacting the metal plating layer and forming an insulating layer overlying said lower structure, and contacting the metal plating layer and having at least one through opening extending to said lower conductor structure; and

forming an upper conductor structure which also includes a metal plating layer on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

wherein each said step of forming a conductor structure is carried out by:

forming at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide, or a conductive oxide film; and

performing a plating operation in order to form ~~a~~ the metal plating layer on the at least one layer, so that the metal plating layer adheres to the at least one layer; and

wherein said steps of forming a lower conductor structure and an upper conductor structure are carried out so that the at least one layer of the upper conductor structure contacts the metal plating layer of the lower conductor structure.

Claim 27 (Showing Amendments that should have been Made)

27. A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region, a gate wiring, a lower conductor structure which includes a metal plating layer, and an insulating layer overlying said lower structure, and contacting the metal plating layer and having at least one through opening extending to said lower conductor structure; and

forming an upper conductor structure on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

wherein said step of forming an upper conductor structure is carried out by:

forming at least one layer of a metal, a

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15	metal silicide, a metal nitride, a metal carbide, or a
16	conductive oxide film;
17	performing a plating operation in order to
18	form a metal plating layer on the at least one layer, so
19	that the metal plating layer adheres to the at least one
20	layer; and
21	after said step of performing a plating
22	operation, performing a thermal treatment in order to
23	diffuse material from the plating layer into the at least
24	one layer.

	Issued Claim 2 (Showing Amendments that were actually Made)
1	3. A method of fabricating a semiconductor device,
2	comprising the steps of:
3	providing a substrate having a doped
4	semiconductor region, a gate wiring, a lower conductor
5	structure which includes a metal plating layer, and an insulating layer overlying said lower
6	structure and contacting metal plating layer and having at least one through opening
7	extending to said lower conductor structure; and
8	forming an upper conductor structure on the
9	insulating layer and causing the upper conductor
10	structure to be connected to the lower conductor
11	structure via the through opening;
12	wherein said step of forming an upper conductor
13	structure is carried out by:
14	forming at least one layer of a metal, a
15	metal silicide, a metal nitride, a metal carbide, or a
16	conductive oxide film;
17	performing a plating operation in order to
18	form a metal plating layer on the at least one layer, so
19	that the metal plating layer adheres to the at least one
20	layer; and
21	after said step of performing a plating
22	operation, performing a thermal treatment in order to
23	diffuse material from the plating layer into the at least
24	one layer.

Thus, with respect to claim 1, the amendments on lines 5, 8 and 16 were correctly entered. In particular, the amendment to line 5 was in accordance with applicant's April 29 amendment and the amendments to lines 8 and 16 were in

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accordance with the Examiner's April 16 amendment. However, the amendment to line 4, which should have been an insertion of "which includes a metal plating layer", in accordance with the Examiner's April 16 amendment, instead is "and contacting the metal plating layer". Moreover, the phrase is inserted following a comma, rather than directly after the word "structure" as directed by the Examiner's amendment. Finally, applicant has also noted that a comma was incorrectly inserted following the word "region" in line 3.

With respect to claim 2, line 5 was correctly amended in accordance with the Examiner's April 16 amendment. However, the amendment to line 6 should have been an insertion of ", and contacting the metal plating layer" in accordance with applicant's April 29 amendment, as was done in line 5 of claim 1. Instead, the phrase "and contacting metal plating layer" was erroneously inserted from the Examiner's April 16 amendment. This phrase lacks proper antecedent basis for "metal plating layer" and was modified by applicant's April 29 amendment.

In view of the above, the following corrections to claims 1 and 2 are necessary to effect the amendments that should have been made and that are clearly disclosed and present in the records of the office. Since the corrections are being made to the issued patent, the claims are set forth below using the line divisions and line numbering from the issued patent:

	CORRECTIONS TO ISSUED CLAIM 1
1	1. A method of fabricating a semiconductor device,
2	comprising the steps of:
3	providing a substrate having a doped semiconductor
4	region[[,]] and a gate wiring, forming a lower conduc-
5	tor structure~~, and contacting the~~ which includes a metal plating
6	layer, and forming an insulating layer overlying
7	said lower structure, and contacting the metal plat-
8	ing layer and having at least one through opening
9	extending to said lower conductor structure; and
10	forming an upper conductor structure which also
11	includes a metal plating layer on the insulating
12	layer and causing the upper conductor structure to
13	be connected to the lower conductor structure via
14	the through opening;
15	wherein each said step of forming a conductor struc-
16	ture is carried out by:
17	forming at least one layer of a metal, a metal sili-

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cide, a metal nitride, a metal carbide, or a conductive oxide film; and

performing a plating operation in order to form the metal plating layer on the at least one layer, so that the metal plating layer adheres to the at least one layer; and

wherein said steps of forming a lower conductor structure and an upper conductor structure are carried out so that the at least one layer of the upper conductor structure contacts the metal plating layer of the lower conductor structure.

CORRECTIONS TO ISSUED CLAIM 2

2. A method of fabricating a semiconductor device, comprising the steps of:

providing a substrate having a doped semiconductor region, a gate wiring, a lower conductor structure which includes a metal plating layer, and an insulating layer overlying said lower structure, and contacting the metal plating layer and having at least one through opening extending to said lower conductor structure; and

forming an upper conductor structure on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

wherein said step of forming an upper conductor structure is carried out by:

forming at least one layer of a metal, a metal silicide, a metal nitride, a metal carbide, or a conductive oxide film;

performing a plating operation in order to form a metal plating layer on the at least one layer, so that the metal plating layer adheres to the at least one layer; and

after said step of performing a plating operation, performing a thermal treatment in order to diffuse material from the plating layer into the at least one layer.

Thus, the following corrections are necessary and are set forth in the attached Certificate of Correction form PTO/SB/44:

Claim 1, line 4, delete --,-- (comma) following "region".

Claim 1, line 5, replace ", and contacting the" with --which includes a--.

Claim 1, line 6, insert --,-- (comma) after the first occurrence of "layer".

Claim 2, line 6, insert --,-- (comma) after "structure".

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Claim 2, line 7, insert --the-- following "contacting".

Conclusion

Applicant has established that these errors were incurred through the fault of the office and are clearly disclosed in the records of the office. Morever, the enclosed documentation (Exhibits A-F) unequivocally supports the patentee's assertions. Accordingly, a Certificate of Correction should be expeditiously issued.

Since this Certificate of Correction is necessitated by a Patent Office error, no fee is required. However, if a fee is required, please charge it to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: July 28, 2006

By:________________________
Troy M. Schmelzer
Registration No. 36,667
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 5,342,806

DATED : August 30, 1994

INVENTOR(S): Michio ASAHINA

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Claim 1, line 4, delete --,-- (comma) following "region".

Claim 1, line 5, replace ", and contacting the" with --which includes a--.

Claim 1, line 6, insert --,-- (comma) after the first occurrence of "layer".

Claim 2, line 6, insert --,-- (comma) after "structure".

Claim 2, line 7, insert --the-- following "contacting".

MAILING ADDRESS OF SENDER: Troy M. Schmelzer, Reg. No. 36,667
Hogan & Hartson LLP
500 S. Grand Ave., Suite 1900
Los Angeles, CA 90071

PATENT NO. 5,342,806

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